UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/781,492	02/13/2001	Magdy S. Abadir	SC11403TS	9497

23125 7590 06/29/2004

FREESCALE SEMICONDUCTOR, INC.
LAW DEPARTMENT
7700 WEST PARMER LANE MD:TX32/PL02
AUSTIN, TX 78729

EXAMINER	
THOMPSON, ANNETTE M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/781,492	ABADIR ET AL.	
	Examiner	Art Unit	
	A. M. Thompson	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-15,17-22 and 24-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-15,17-22 and 24-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11 December 2003 has been entered.

2. The declarations under 37 CFR 1.132 filed October 9, 2003 and November 7, 2003 are sufficient to overcome the 35 U.S.C. 102 (a) rejections of claims 8-10, 12-15, 17, 19-22, and 24-31 as anticipated by the Bhadra paper.

3. Although the declarations are persuasive, new grounds of rejection are herein entered. Claims 8-15, 17-22, and 24-31 are pending.

Drawings

4. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Obj ctions

5. Applicant is advised that should claim 11 be found allowable, claim 21 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

6. Claim 24 is objected to because of the following informalities: Pursuant to claim 24, "capable of" is considered precatory language and should be replaced with a more definite recitation, e.g. "that identifies" or "which identifies", or some similar phraseology. Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 13-15, 17-20 and 24-31 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Although the claims provide enablement for an ATPG tool, the claims do not disclose the ATPG tool as having an ATPG model.

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 14, 18 and 24-31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Additionally, pursuant to claims 14 and 25, Applicants recite "translating the first set of paths", however, it is unclear what Applicants mean by "translating". Although Applicants' Figure 3 discloses this term, Applicants' specification does not further clarify. Pursuant to claim 18, Applicants' specification indicates that the false path report is fed back to *a timing analysis procedure*, not a static analysis tool and this limitation is interpreted in accordance with Applicants' specification. Pursuant to claim 24, Applicants' specification is not specifically directed towards disclosing a method for interfacing between a static analysis tool and an ATP tool.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Rejection of claims 8-15, 17-22, 24-31

12. Claims 8-15, 17-22, 24-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Kunda et al. (Kunda), U.S. Patent 5,675,728. Kunda discloses an apparatus and method identifying false timing paths in digital circuits.

13. Pursuant to claim 8, Kunda discloses [a] method for identifying false paths, comprising providing a path corresponding to a circuit design (col. 2, ll. 8-10); determining whether a set of final value conditions are satisfied (col. 2, ll. 14-16); determining whether a set of side value propagation conditions are satisfied (col. 2, ll. 12-14); determining whether a set of initial value conditions are satisfied (co. 2, ll. 39-42); determining whether the path is false based on at least one of the set of final value conditions, the set of side values propagation conditions, and the set of initial value conditions (col. 2, ll. 17-21; col. 2, ll. 43-47).

14. Pursuant to claim 9, further comprising determining whether a set of slower path conditions are satisfied, and wherein determining whether the path is false is based on at least one of the set of final value conditions, the set of side value propagation conditions, and the set of initial value conditions, and the set of slower path conditions (col. 8, ll. 20-38).

15. Pursuant to claim 10, wherein the set of final value conditions and the set of side value propagation conditions correspond to a first time frame and the set of initial value conditions correspond to a second time frame different from the first time frame (col. 4, line 63 to col. 5, line 14).

16. Pursuant to claim 11, Kunda discloses a method for identifying false paths (Abstract) comprising providing a first set of paths corresponding to the circuit design, the first set of paths having single-path component logic blocks and multiple-path component logic blocks (Fig. 6A; col. 4, ll. 63-67); extracting a second set of paths from the first set of paths, the second set of paths having no multiple-path component logic

blocks (Fig. 6B); providing a path corresponding to a circuit design (col. 2, ll. 8-10) by selecting the path from the second set of paths; determining whether a set of final value conditions are satisfied (col. 2, ll. 14-16); determining whether a set of side value propagation conditions are satisfied (col. 2, ll. 12-14); determining whether a set of initial value conditions are satisfied; and determining whether the path is false based on at least one of the set of final value conditions, the set of side value propagation conditions, and the set of initial value conditions (col. 2, ll. 17-21; col. 2, ll. 43-47).

17. Pursuant to claim 12, wherein at least one of determining whether a set of final value conditions are satisfied, determining whether a set of side value propagation are satisfied, and determining whether a set of initial value conditions are satisfied, is performed by an automatic test pattern generation tool (Fig. 2, #208; col. 4, ll. 19-29; col. 8, ll. 8-19).

18. Pursuant to claim 13, Kunda discloses a method for false path identification within a circuit design (Abstract) comprising receiving a first set of paths corresponding to the circuit design (col. 4, ll. 63-67); providing a set of conditions corresponding to at least one path of the first set of paths to an ATPG tool (col. 4, ll. 35-29), the ATPG tool having an ATPG model corresponding to at least a portion of the circuit design, the set of conditions comprising whether a final value condition is satisfied, whether one or more side value propagation conditions are satisfied, whether an initial value conditions is satisfied, and whether one or more slower path conditions are satisfied (col. 4, ll. 11-21); the ATPG tool generating a response to the set of conditions using the ATPG

model (Fig. 2, #209); and identifying a false path within the first set of paths based on the response from the ATPG tool (col. 4, ll. 46-51).

19. Pursuant to claim 14, further comprising after receiving the first set of paths, translating the first set of paths (col. 2, ll. 36-39, propagating test signals along the paths).

20. Pursuant to claim 15, further comprising after receiving the first set of paths, extracting a second set of paths from the first set of paths, wherein the set of conditions corresponds to at least one path of the second set of paths (col. 5, ll. 15-28).

21. Pursuant to claim 17, wherein the response to the set of conditions from the ATPG tool indicates whether the set of conditions is satisfied (Fig. 2, #209; col. 4, ll. 25-51; col. 8, ll. 19-38; see also Applicants' admission in specification, page 18, lines 21-23).

22. Pursuant to claim 18, Kunda discloses a method for false path identification within a circuit design (Abstract) comprising receiving a first set of paths corresponding to the circuit design (col. 4, ll. 63-67) from a static analysis tool (Admission in Applicants' specification, page 1, lines 10-15); providing a set of conditions corresponding to at least one path of the first set of paths to an ATPG tool (col. 4, ll. 35-29), the ATPG tool having an ATPG model corresponding to at least a portion of the circuit design; the ATPG tool generating a response to the set of conditions using the ATPG model; and identifying a false path within the first set of paths based on the response from the ATPG tool (col. 4, ll. 46-51), wherein a false path report is fed back to a timing analysis tool (col. 4, ll. 41-51).

23. Pursuant to claims 19, wherein the ATPG tool is a commercially available ATPG tool (Admission in Applicants' specification, page 8, lines 19-21).

24. Pursuant to claim 20, wherein receiving the first set of paths comprises receiving the first set of paths from a static analysis tool (Admission in Applicants' specification page 1, lines 10-15).

25. Pursuant to claim 21, it incorporates the limitations already rejected in claim 11 and therefore claim 21 is likewise rejected based on the same reasoning.

26. Pursuant to claim 22, it incorporates the limitations already rejected in claim 9, and therefore claim 22 is likewise rejected based on the same reasoning.

27. Pursuant to claim 24 which recites a method for interfacing between a static analysis tool and an ATPG tool (see Fig. 2) that identifies false paths within a circuit design comprising receiving a first set of paths corresponding to the circuit design (col. 4, ll. 63-67); providing a set of conditions corresponding to at least one path of the first set of paths to the ATPG tool (col. 4, ll. 35-29); receiving a response to the set of conditions generated by the ATPG tool using the ATPG model (Fig. 2, #209); and identifying a false path within the first set of paths based on the response from the ATPG tool (col. 4, ll. 46-51).

28. Pursuant to claim 25, further comprising translating the first set of paths (col. 2, ll. 36-39, propagating test signals along the paths), after receiving the first set of paths.

29. Pursuant to claim 26, further comprising after receiving the first set of paths, extracting a second set of paths from the first set of paths, wherein the set of conditions corresponds to at least one path of the second set of paths (col. 5, ll. 15-28).

30. Pursuant to claim 27 wherein the set of conditions comprises at least one of final value conditions, initial value conditions, side propagation value conditions, and slower path conditions (col. 8, ll. 20-38).

31. Pursuant to claim 28, wherein the response to the set of conditions from the ATPG tool indicates whether the set of conditions is satisfied (Fig. 2, #209; col. 4, ll. 25-51; col. 8, ll. 19-38; see also Applicants' admission in specification, page 18, lines 21-23).

32. Pursuant to claim 29, further comprising providing a false path report to a timing analysis tool (col. 4, ll. 41-51).

33. Pursuant to claim 30, wherein the ATPG tool is a commercially available ATPG tool (Admission in Applicants' specification, page 8, lines 19-21).

34. Pursuant to claim 31, wherein the first set of paths is received from the static analysis tool (Admission in Applicants' specification page 1, lines 10-15).

Conclusion

35. Any inquiry concerning this communication or earlier communications should be directed to Examiner A.M. Thompson whose telephone number is (571) 272-1909. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 4:30 p.m.. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matthew S. Smith, can be reached on (571) 272-1907.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

36. Responses to this action should be mailed to the appropriate mail stop:

Mail Stop _____
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to:

(703) 872-9306, (for all **OFFICIAL** communications intended for entry)

A. M. THOMPSON
Primary Examiner
Technology Center 2800